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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,256	08/27/2003	Yoshihiro Nonaka	8031-1028	5218

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EXAMINER	
NADAV, ORI	
ART UNIT	**PAPER NUMBER**
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,256	NONAKA, YOSHIHIRO	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,8,16-23,31 and 32* is/are pending in the application.

4a) Of the above claim(s) *5,8 and 16-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (6,99,516) or Wirth et al. (5,270,657) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 2 and 31-32, Aoki et al. teach in figures 6 and 12 and related text a semiconductor integrated circuit comprising:

at least four power supply lines V1-V4; and

at least two transistors Q1-Q3 for switching between said at least four power supply lines,

wherein the first, second and third power supply lines of said at least four power supply lines are arranged side by side in said order,

and said at least two transistors include first and second transistors respectively placed in the gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors are formed on the opposite sides of said second power supply line;

wherein at least one of said power supply lines extends straight to be connected to an external connection terminal.

Aoki et al. do not teach using the transistors as thin-film transistors formed on an insulation substrate other than a glass substrate or a semiconductor substrate, and wherein said first transistor switches between said first and second power supply lines and said second transistor switches between said second and third power supply lines.

Regarding claims 2 and 31-32, Wirth et al. teach in figure 13 and related text a semiconductor integrated circuit comprising:

at least four power supply lines 151-154; and

at least two transistors for switching between said at least four power supply lines,

wherein the first, second and third power supply lines of said at least four power supply lines are arranged side by side in said order,

and said at least two transistors include first and second transistors respectively placed in the gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors are formed on the opposite sides of said second power supply line, and

wherein said first transistor switches between said first and second power supply lines and said second transistor switches between said second and third power supply lines, and

wherein at least one of said power supply lines extends straight to be connected to an external connection terminal.

Wirth et al. do not teach using the transistors as thin-film transistors formed on an insulation substrate other than a glass substrate or a semiconductor substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the transistors as thin-film transistors formed on an insulation substrate other than a glass substrate or a semiconductor substrate, and wherein said first transistor switches between said first and second power supply lines and said second transistor switches between said second and third power supply lines, in the device of Aoki et al. or Wirth et al., in order to use the device in an application which requires thin-film transistors formed on an insulation substrate other than a glass substrate or a semiconductor substrate, wherein said first transistor switches between said first and second power supply lines and said second transistor switches between said second and third power supply lines.

Regarding the claimed limitations of first and second transistors respectively placed in the gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors are formed on the opposite sides of said second power supply line, although Aoki et al. or Wirth et al. do not explicitly state that the first and second transistors respectively placed in the gap between said first and second power supply lines and a gap between said second and third power supply lines, said first and second transistors are formed on the opposite

sides of said second power supply line, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place first and second transistors respectively in the gap between said first and second power supply lines and a gap between said second and third power supply lines, and said first and second transistors on the opposite sides of said second power supply line, in the device of Aoki et al. or Wirth et al., in order to follow the illustrations depicted in the corresponding drawings.

Regarding claim 4, AAPA teaches in figure 34 that the area occupied by all of said power supply lines is larger than the area occupied by all of the regions between said power supply lines. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the area occupied by all of said power supply lines larger than the area occupied by all of the regions between said power supply lines in prior art's device in order to reduce the size of the device.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., Wirth et al. and AAPA, as applied to claim 31 above, and further in view of Fujii et al. (6,707,139).

Aoki et al., Wirth et al. and AAPA teach substantially the entire claimed structure, as applied to claim 1 above, except a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is

not connected to any of said power supply lines other than those having equal potentials.

Fujii et al. teach in figure 8 and related text a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is not connected to any of said power supply lines other than those having equal potentials.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a mutual connection line for connecting together some of said power supply lines having equal potentials, wherein the mutual connection line is not connected to any of said power supply lines other than those having equal potentials, in the device of Aoki et al., Wirth et al. and AAPA, in order to use the device in an application which requires power supply lines of equal potentials.

Response to Arguments

Applicant argues that prior art teaches the circuit diagrams of the claimed invention, and does not teach the layout of the transistors and the power supply lines.

The rejected claims do not recite "A layout of a semiconductor device". In fact, the rejected claims recite "A semiconductor integrated circuit". Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Note that the broad recitation of the claim does not require the arrangement of the transistors and the power supply lines to be in a "planar layout when viewed from above"

Applicant argues that prior art does not teach using the transistors to switch the power supply lines.

Wirth et al. teach in the abstract using the transistors as switch mode amplifiers. Although Aoki et al. do not teach using the transistors to switch the power supply lines, AAPA (the secondary reference) teaches using the transistors to switch the power supply lines.

Note further that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
12/12/06

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